The First Very Low-IF RX, 2-Point Modulation TX CMOS System On Chip Bluetooth Solution

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Abstract — The proposed low cost Bluetooth single-chip solution is implemented in a 0.25μm CMOS technology. The "System On Chip (SOC)" includes all necessary baseband- and RF-parts to achieve full Bluetooth functionality, by occupying 18.5mm^2 chip area in total. The maximum current consumption of the analog part is 60mA. The internal regulated supply voltages of the analog and digital parts are 2.65V. First measurement results of basic functionalities are discussed in this paper.

I. Introduction

The new short range communication standard Bluetooth™ [1, 2, 3] enables the networking of devices like mobile phones, laptops, palmtops etc. in the unlicensed 2.4GHz ISM band. Low cost, low power consumption and small feature size are the main design issues for Bluetooth interfaces. The used CMOS technology allows the integration of baseband and RF-part on the same die, which minimizes cost and size. A careful floorplanning, layout arrangements, isolation concepts, system architecture and circuit design are combined to achieve an optimum isolation between these parts. Two completely independent and separately located voltage regulators minimize the digital crosstalk via the power supplies to the analog RF-parts. Only for the VCO a coil is implemented, for the LNA an inductorless architecture is chosen. This prevents inductive crosstalk among transmit and receive path, and reduces size. Closed loop modulation, and the earliest reasonable change to the digital domain in the receiver, result in a robust, crosstalk insensitive system solution. The single-chip is highly integrated (>1e6 transistors) and realizes most of the system functions needed for communication under the Bluetooth standard. The single-chip system incorporates the transceiver for the 2.4GHz ISM frequency band, with an on-chip TXA-driver, a fully differential LNA and channel select filter. Together with the Bluetooth software "ProBlue", which incorporates the Host Controller Interface (HCI) and Link Manager (LM), a system for Bluetooth wireless technology can be developed. To compose the complete hardware for a Bluetooth interface only a few external (passive) components are needed. Thus the main design issues for Bluetooth interfaces are attained with the proposed "CMOS System On Chip Bluetooth Solution".

II. Architecture

The proposed low cost single-chip architecture is depicted in Fig. 1, baseband and RF-part will be discussed in detail below.

A. Digital Part

The baseband part can be divided into the digital baseband section, the analog baseband section, and the Link Control section.

Within the digital baseband section the demodulation unit is located, as well as the digital part of the ΣΔ-Fractional-N-PLL, and the control logic for the analog RF section, including time-, power- and GFSK-modulation-control for the PLL. An amplitude tunable Gaussian impulse filter is implemented, to achieve the matching between the two modulation paths of the ΣΔ-Fractional-N-PLL.

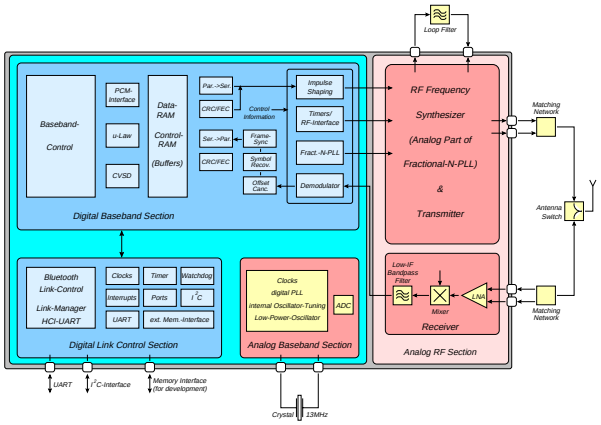

Fig. 1: Bluetooth SOC block diagram.

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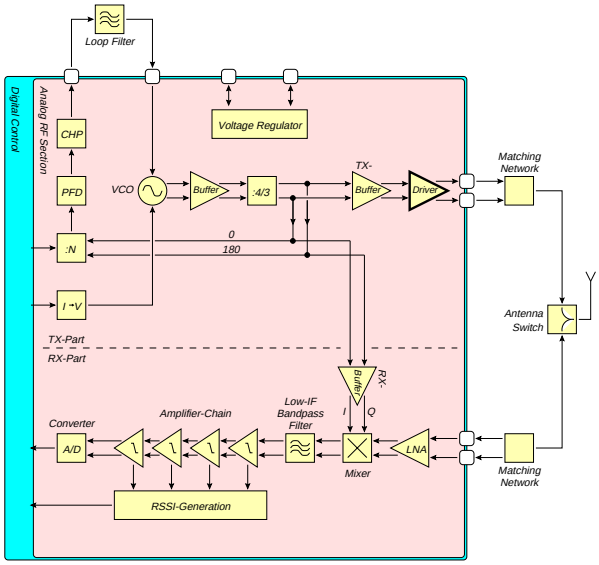

Fig. 2: Block diagram of the analog RF-part.

In the analog baseband section a 8bit A/D converter for the RSSI information from the receiver, the 13MHz crystal oscillator, its associated clock generation, and the voltage regulator for the digital power supply are placed.

The Link Control section includes the Link Control Management unit, and several I/O interfaces for application flexibility (4-wire PCM interface, UART, I^2C interface, memory interface). During startup the digital control reads the configuration information from the external E^2PROM, like crystal adjustment, the Bluetooth device address etc. All other functions are done via HCI-UART. Therefore no hardware specific firmware or software development has to be done.

B. Analog RF-Part

The analog section is depicted more detailed in Fig. 2. It is divided into the TX- and the RX-part. In the TX-part a 2-Point closed loop modulation scheme is used to achieve the 1Mbit/s 2-GFSK modulation. The gauss filtered data are injected into the loop via a low- and a high-frequency modulation path. The low-frequency modulation path is controlled by the $\Sigma\Delta$-Fractional-N-synthesizer and is defined by the loop bandwidth. The noise shaping characteristic of the $\Sigma\Delta$-converter [4] allows the shift of low frequency noise to higher frequencies, where it is attenuated by the loop filter. The high-frequency modulation is injected into the loop by direct VCO modulation. Separate voltage dependent capacitors within the VCO are used for VCO tuning and modulation. The 13MHz on-chip crystal oscillator provides the digital clock frequency and the reference for the phase-frequency detector (PFD). The VCO operates at 4/3 of the nominal transmitter frequency, to avoid VCO pulling due to the output driver. The conversion to 2.4GHz is achieved with an up-conversion image reject mixer. A passive polyphase filter performs the 0° and 90° phase shift for the mixer [5].

For equitable integration of the channel select filter a low-IF receiver architecture [6] is chosen. The 1MHz IF allows an AC-coupling between the amplifier stages to remove static and dynamic DC offsets, without affecting the desired signal. The receiver is implemented fully differential to reduce the influence of switching noise from the digital circuits. Because of the low cross talk sensitivity, the LNA (Fig. 3) is implemented as an inductorless cascoded differential amplifier. A mixture of resistive and capacitive feedback is used to achieve a resistive input impedance. An external balun (matching network) is needed for the single-ended to differential conversion of the antenna signal.

The RF-signal is down converted into the near Zero-IF region of 1MHz by an I/Q mixer. A 5^{th} order automatic adjusted polyphase filter is implemented for channel select filtering in the complex-domain. Due to the balanced design of the I/Q mixer, the LO-path, and the polyphase filter, an image rejection of $>$20dB is provided. The signals are amplified by a chain of AC-coupled amplifiers, until they become clipped. The total gain of the amplifier chain is 80dB. The analog representation of the RSSI signal is generated from the outputs of the first amplifiers and A/D-converted for further digital processing. The dynamic range of the RSSI signal is 55dB. A self calibrating biasing is used in each amplifier stage, to reduce static and dynamic offsets. The clipped differential signal at the end of the amplifier chain is A/D-converted and demodulated in the digital part.

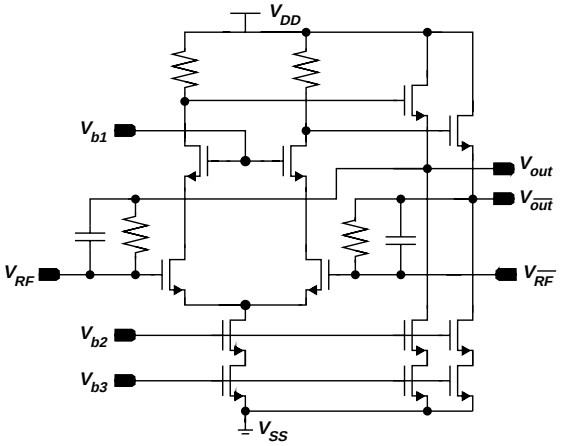

Fig. 3: Schematic of the inductorless LNA.

Fig. 4 shows the chip photo of the entire single-chip. The total chip area is 18.5mm^2. The baseband part covers roughly $3/4$, and the RF-part $1/4$ of the entire chip area. A careful floorplanning and the use of guard rings and shieldings provide the optimum isolation between the analog and digital part.

III. Measurements

First measurement results indicate good function of all implemented analog and digital functional blocks. Successful bidirectional data transfers between the Bluetooth single-chip and other listed Bluetooth transceivers over a distance of >14m point out the functioning of the proposed concept.

As shown in Fig. 5 the digitally controlled Fractional-N-PLL locks at the 79 Bluetooth channels, by achieving a channel independent phase noise of -124dBc/Hz at 3MHz offset. The measured and simulated VCO characteristics are shown in Fig. 6. Except for a small offset, simulations and measurements are in good agreement.

The Gaussian shape of the demodulated, transmitted signal, shown in Fig. 7, indicates the wanted interaction of the two PLL modulation paths. The TXA-driver provides an output power of 0dBm. For higher power levels an optional external PA can be used.

The minimum detectable receiver signal is -74dBm at 0.1% BER, which is 4dB higher than required. In a further redesign the sensitivity will be improved by reducing parasitic capacitances in the LO path. The measured in-band blocker rejection is pictured in Fig. 8. The minimum margin to the Bluetooth receiver interference specification is 4dB for the co-channel, which is set by the demodulator capture range. The adjacent channel rejection is set by the roll-off of the channel-select filter. The image rejection is 28-29dB, nearly 10dB better than specified in the Bluetooth standard. In Fig. 9 the measured AC-response of the 5th order polyphase filter can be seen. After passing the automatic adjustment cycles the AC-response of the filter meets exactly the wanted characteristics. Furthermore the available tuning range of the filter corner frequencies indicates that fabrication tolerances can easily be balanced.

The maximum current consumption of the analog part is 60mA. The implementation of an inductorless receiver is in fact more power consumptive than recent solutions reported before. The benefit of this approach is the low cross talk sensitivity and the smaller size, which simplifies a Bluetooth single-chip solution. The relatively high current consumption is also caused by the choice of higher tail currents than required, to ensure the functionality of the first realization. The supply voltage of digital and analog part is 2.65V, both are internal regulated.

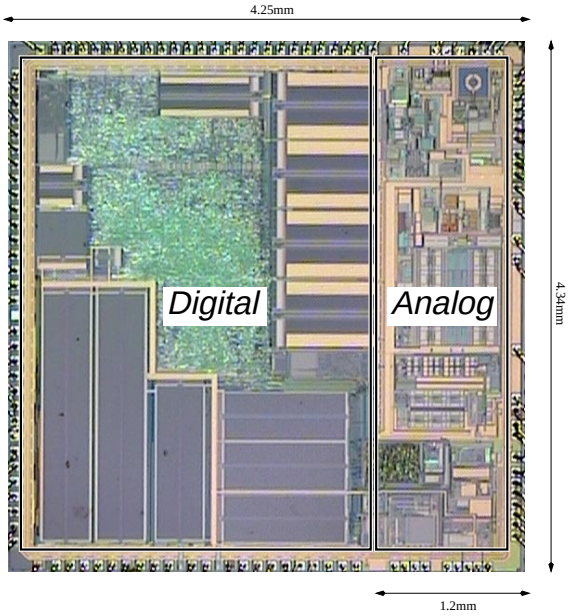

Fig. 4: Chip photo of the single-chip.

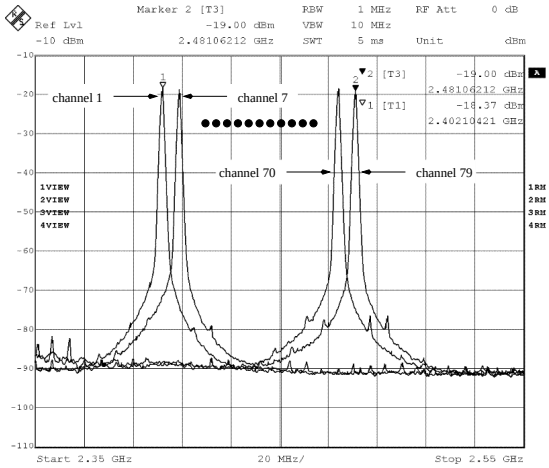

Fig. 5: Controlled 3/4-frequency of the VCO.

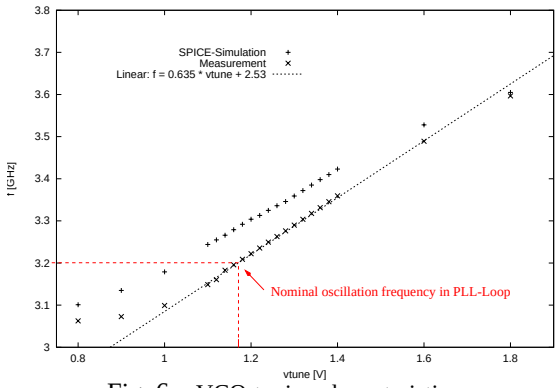

Fig. 6: VCO-tuning characteristic.

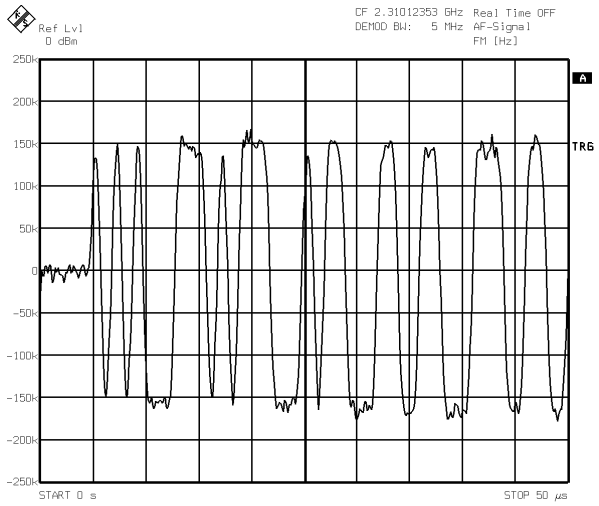

Fig. 7: Demodulated, transmitted Gauss impulse sequence.

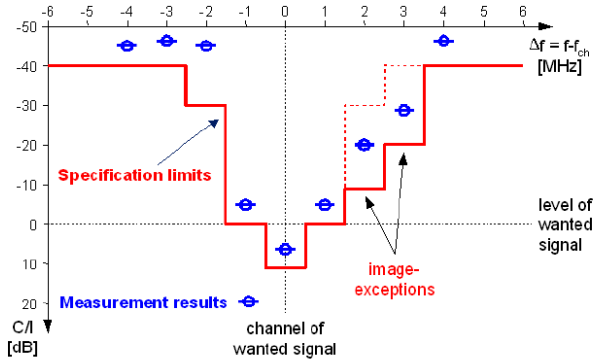

Fig. 8: Receiver interferer performance at 0.1% BER.

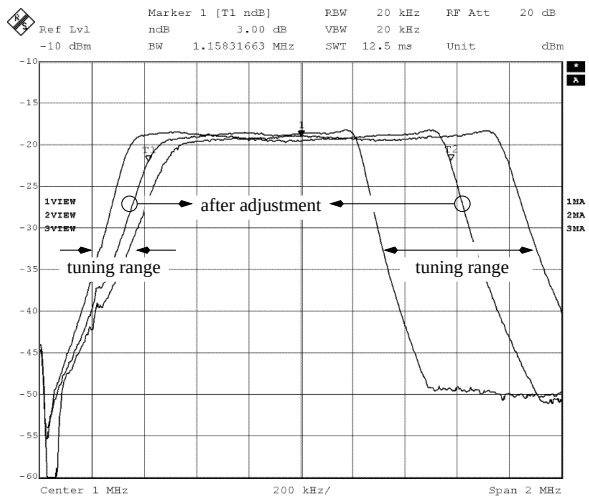

Fig. 9: AC-response of the 5th order polyphase filter.

IV. Conclusion

A low cost concept for a "CMOS System On Chip Bluetooth Solution" has been presented. The measurement results meet the Bluetooth specifications and show the suitability of the presented single-chip concept. Crosstalk between the analog and digital parts is the drawback of single-chip solutions. This effect is kept small by the proposed crosstalk insensitive system concept, circuit design and layout. In a further redesign the current consumption of the baseband and RF-part will be reduced and the receiver sensitivity increased. Due to the need of only a few external elements, a chip size of 18.5mm^2, and a reasonable power consumption, the proposed single-chip solution fulfills the main design issues for small size, low cost Bluetooth interfaces. Within the next redesign step full Bluetooth performance and a reduced power consumption will be achieved.

Acknowledgment

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References

[1] *Bluetooth™ – is a trademark owned by its proprietor and used by Infineon Technologies AG under license*, 1999 – 2000.

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